HI5667EVAL2 Evaluation Board User's Manual

Application Note | August 1999 | AN9854

Description

The HI5667EVAL2 evaluation board allows the circuit designer to evaluate the performance of the Intersil HI5667 monolithic 8-bit 60MSPS analog-to-digital converter (ADC). As shown in the Evaluation Board Functional Block Diagram, the evaluation board includes sample clock generation circuitry, a single-ended to differential analog input RF transformer configuration, an on board external variable reference voltage generator and a digital data output header/connector. The digital data outputs are conveniently provided for easy interfacing to a ribbon connector or logic probes. In addition, the evaluation board includes some prototyping area for the addition of user designed custom interfaces or circuits.

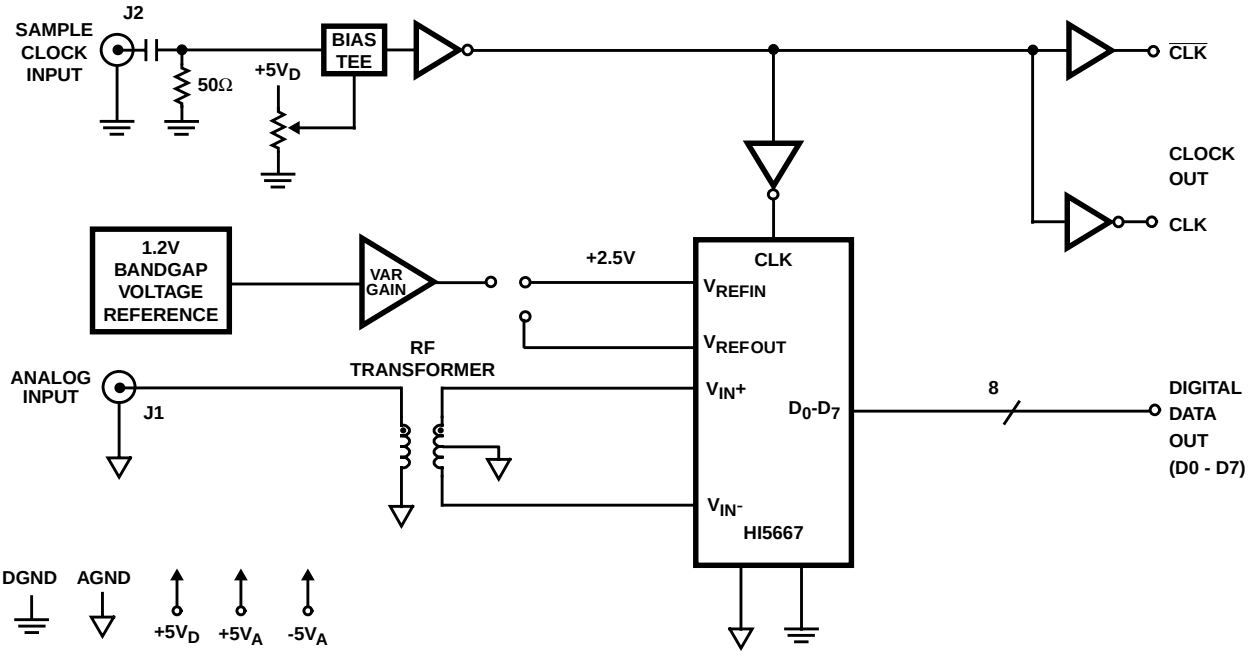
The sample clock generator circuit accepts the external sampling signal through an SMA type RF connector, J2. This input is AC-coupled and terminated in 50Ω allowing for connection to most laboratory signal generators. In addition, the duty cycle of the clock driving the A/D converter is adjustable by way of a potentiometer. This allows the effects of sample clock duty cycle on the HI5667 to be observed.

The analog input signal is also connected through an SMA type RF connector, J1, and applied to a single-ended to differential analog input RF transformer. This input is AC-coupled and terminated in 50Ω allowing for connection to most laboratory signal generators.

The converters' digital data outputs along with two phases of the sample clock (CLK and $\overline{CLK}$) are provided at the output header/connector. With this output configuration the digital data output transitions seen at the I/O header/connector are essentially time aligned with the rising edge of the sampling clock (CLK) or the falling edge of the out of phase sampling clock ($\overline{CLK}$).

Refer to the component layout and the evaluation board electrical schematic for the following discussions.

Evaluation Board Functional Block Diagram



External Reference Voltage Generator, V_{REFOUT} and V_{REFIN}

The HI5667 has an internal reference voltage generator, therefore no external reference voltage is required. The evaluation board, however, offers the ability to use the converters' internal reference voltage, V_{REFOUT}, or the on board external variable reference voltage generator.

The external variable reference voltage circuitry is implemented using the Intersil ICL8069 low voltage, 1.2V, bandgap reference (D1) sourcing a non-inverting variable gain operational amplifier circuit based on the Intersil HA5127 ultra-low noise precision operational amplifier (U1). Potentiometer VR1 is used to adjust the output voltage level of this external voltage reference. With this the user is able to observe the effects of reference voltage variations on the converters performance. Turning VR1 in a clockwise (CW) direction will decrease the external reference voltage while turning VR1 in a counterclockwise (CCW) direction will decrease the external reference voltage.

Selection of the reference voltage to be used by the converter is accomplished by placing the P3 header jumper across the appropriate pins. The converters' internal reference voltage generator, V_{REFOUT}, must be connected to V_{REFIN} when using the converters internal reference and is selected by placing the P3 header jumper across P3-2 and P3-3. Alternately, if it is desired to use the on board external variable reference voltage generator, selection of this option is done by placing the P3 header jumper across P3-1 and P3-2. See Appendix A, Board Layout for the location of the P3 reference voltage selection header.

Analog Input

The fully differential analog input of the HI5667 A/D can be configured in various ways depending on the signal source and the required level of performance.

Differential Analog Input Configuration

A fully differential connection (Figure 1) will yield the best performance from the HI5667 A/D converter. Since the HI5667 is powered off a single +5V supply, the analog input must be biased so it lies within the analog input common mode voltage range of 0.25V to 4.75V. Figure 2 illustrates the differential analog input common mode voltage, VDC,

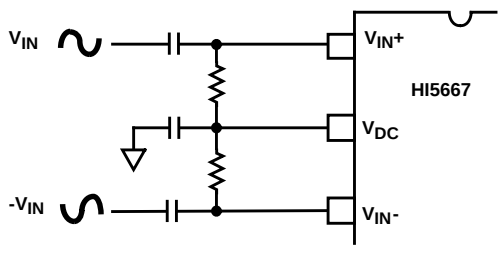


FIGURE 1. AC COUPLED DIFFERENTIAL INPUT

range that the converter will accommodate. The performance of the converter does not change significantly with the value of the analog input common mode voltage.

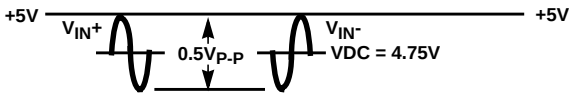


FIGURE 2A.

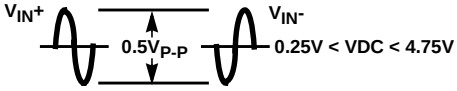


FIGURE 2B.

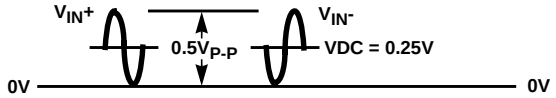


FIGURE 2C.

FIGURE 2. DIFFERENTIAL ANALOG INPUT COMMON MODE VOLTAGE RANGE

A DC bias voltage source, V_{DC}, equal to 3.0V (typical), is made available to the user to help simplify circuit design when using an AC coupled differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent DC bias source and stays well within the analog input common mode voltage range over temperature.

For the AC coupled differential input (Figure 1) and with V_{REFIN} connected to V_{REFOUT}, full scale is achieved when the V_{IN} and $-V_{IN}$ input signals are $0.5V_{P-P}$, with $-V_{IN}$ being 180 degrees out of phase with V_{IN}. The converter will be at positive full scale when the $V_{IN}+$ input is at V_{DC} + 0.25V and the $V_{IN}-$ input is at V_{DC} - 0.25V ($V_{IN}+ - V_{IN}- = +0.5V$). Conversely, the converter will be at negative full scale when the $V_{IN}+$ input is equal to V_{DC} - 0.25V and $V_{IN}-$ is at V_{DC} + 0.25V ($V_{IN}+ - V_{IN}- = -0.5V$).

It should be noted that overdriving the analog input beyond the ±0.5V full scale input voltage range will not damage the converter as long as the overdrive voltage stays within the converters analog supply voltages. In the event of an overdrive condition the converter will recover within one sample clock cycle.

A single-ended input will give better overall system performance if it is first converted to differential before driving the HI5667. An RF transformer can be connected to the HI5667 input to provide the single-ended to differential conversion. The particular transformer used will depend on the input voltage level, the impedance desired, and the input frequency range. The transformer will tend to have a bandpass response resulting in low and high frequency

cutoffs. This is the type of single-ended to differential conversion circuitry that is provided on the HI5667EVAL2 evaluation board (refer to the HI5667EVAL2 evaluation board parts layout and the electrical schematics).

The HI5667EVAL2 evaluation board provides the single-ended to differential analog front-end for converting the typical laboratory signal generators 50Ω single-ended output to a differential input signal for the converters differential-in-differential-out sample-and-hold front end. The input of this analog front-end, RF SMA connector J1, is AC coupled and provides a termination impedance of 50Ω.

The Mini-Circuits T4-1 transformer, T1, provides a 1dB passband from 2MHz to 100MHz. Since this transformer has a 1:4 primary to secondary impedance ratio the 200Ω secondary impedance, created by the series resistance of R9 and R10, is now transformed to 50Ω at the transformer primary side (200/4 = 50).

Alternate transformers could be used with minor modifications to the input circuit. For example, if one desired a narrower input frequency range than that provided by the Mini-Circuits T4-1 transformer one could replace the T4-1 with a Mini-Circuits TMO2.5-6T. The TMO2.5-6T transformer provides a 1dB passband from 0.05MHz to 20MHz and has a 1:2.5 primary to secondary impedance ratio. With this, the 200Ω secondary load (two 100Ω resistors, R9 and R10, connected across the transformer secondary) is now transformed to 80Ω (200/2.5 = 80) at the transformer primary side input. In order to achieve a 50Ω input impedance at the analog input connector, J1, it would be necessary to install a 130Ω resistor in the R3 (A/R) location, i.e. the impedance now seen looking into the J1 SMA connector is 130Ω (R3) in parallel with 80Ω for an effective impedance of 50Ω.

When using transformer coupling, care should be exercised in the area of impedance matching or undesirable distortion components could result from mismatching and affect the overall measured performance of the converter.

Evaluation Board Layout and Power Supplies

The HI5667 evaluation board is a four layer board with a layout optimized for the best performance of the converter. This application note includes an electrical schematic of the evaluation board, a component parts list, a component placement layout drawing and reproductions of the various board layers used in the board stack-up. The user should feel free to copy the layout in their application.

The HI5667 monolithic A/D converter has been designed with separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The evaluation board provides separate low impedance analog and digital ground planes on layer 2. Since the analog and digital ground planes are connected together at a single point where the power supplies enter the board, **DO NOT** tie them together back at the power supplies.

The analog and digital supplies are also kept separate on the evaluation board and should be driven by clean linear regulated supplies. The external power supplies are hooked up with the twisted pair wires soldered to the plated through holes marked +5VAIN, +5VA1IN, -5VAIN, +5VDIN, +5VD1IN, +5VD2IN, AGND and DGND near the prototyping area. +5VDIN, +5VD1IN and +5VD2IN are digital supplies and are returned to DGND. +5VAIN, +5VAIN1 and -5VAIN are the analog supplies and are returned to AGND. Table 1 lists the operational supply voltages, typical current consumption and the evaluation board circuit function being powered. Single supply operation of the converter is possible but the overall performance of the converter may degrade.

TABLE 1. HI5667EVAL2 EVALUATION BOARD POWER SUPPLIES

POWER SUPPLY	NOMINAL VALUE	CURRENT (TYP)	FUNCTION(S) SUPPLIED
+5VAIN	5.0V ±5%	6mA	External Reference Voltage Operational Amplifier, Bandgap Reference
-5VAIN	-5.0V ±5%	5mA	External Reference Voltage Operational Amplifier
+5VA1IN	5.0V ±5%	50mA	A/D AV_{CC}
+5VDIN	5.0V ±5%	63mA	Sample Clock Generation
+5VD1IN	5.0V ±5%	20mA	A/D DV_{CC1}
+5VD2IN	3.0V ±10%	5mA	A/D DV_{CC2}

Sample Clock Driver

In order to ensure rated performance of the HI5667, the duty cycle of the sample clock should be held at 50% ±5%. It must also have low phase noise and operate at standard TTL levels.

It can be difficult to find a low phase noise generator that will provide a 60MHz squarewave at TTL logic levels. Consequently, the HI5667EVAL2 evaluation board is designed with a logic inverter (U5) acting as a voltage comparator to generate the sampling clock for the HI5667 when a sinewave (<±1.5V) is applied to the AC-coupled, 50Ω terminated CLK input through SMA type RF connector, J2, of the evaluation board. The sample clock sinewave is AC coupled into the input of the inverter and a discrete bias tee is used to bias the sinewave around the trigger level of the inverter's input. A potentiometer (VR2) varies the DC bias voltage added to the sinewave input allowing the user to adjust the duty cycle of the sampling clock to obtain the best performance from the ADC and to evaluate the effects of sample clock duty cycle on the performance of the converter. The trigger level for the sample clock input to the HI5667

converter is approximately 1.5V. Therefore, the duty cycle of the sampling clock should be measured at the 1.5V trigger level of the HI5667 sample clock input pin.

The sinewave to logic level comparator drives a series of additional inverters that provide isolation between the three sample clocks used on the evaluation board. One clock is used to drive the converter sample clock input pin and the other two provide CLK and $\overline{CLK}$ at the data output header/connector, P2. The clock/data relationship at the P2 output connector is as follows. CLK has rising edges aligned with digital data transitions and $\overline{CLK}$ has rising edges aligned mid-bit.

The data corresponding to a particular analog input sample will be available at the digital outputs of the HI5667 after the data latency (7 cycles) plus the HI5667 digital data output delay.

The sample clock and digital output data signals are made available through two connectors contained on the evaluation board. Line drivers are not provided for the digital output data and it should be pointed out that the load presented to the converter digital output data signals, D0 - D9, should not exceed the data sheet CMOS drive limits and a load capacitance of 10pF. The P1 96-pin I/O connector allows the evaluation board to be interfaced to the DSP evaluation boards available from Intersil. The digital output data and sample clock can also be accessed by clipping the test leads of a logic analyzer or data acquisition system onto the header/connector pins of connector P2.

The A/D converters $\overline{OE}$ control input pin allows the digital output data bus of the converter to be switched to a three-state high impedance mode. This feature enables the testing and debugging of systems which are utilizing one or more converters. This three-state control signal is not intended for use as an enable/disable function on a common data bus and could result in possible bus contention issues. The A/D converters $\overline{OE}$ control input pin is controlled by the installation or removal of a shunt, JP1, contained on the evaluation board. Installation of JP1 forces the $\overline{OE}$ control input pin low for normal operation while removal of JP1 allows the digital output data bus of the converter to be switched to a three-state high impedance mode.

HI5667 Performance Characterization

Dynamic testing is used to evaluate the performance of the HI5667 A/D converter. Among the tests performed are Signal-to-Noise and Distortion Ratio (SINAD), Signal-to-Noise Ratio (SNR), Total Harmonic Distortion (THD), Spurious Free Dynamic Range (SFDR) and Intermodulation Distortion (IMD).

Figure 4 shows the test system used to perform dynamic testing on high-speed ADCs at Intersil. The clock (CLK) and analog input (V_{IN}) signals are sourced from low phase noise HP8662A synthesized signal generators that are phase locked to each other to ensure coherence. The output of the signal generator driving the ADC analog input is bandpass filtered to improve the harmonic distortion of the analog input signal. The comparator on the evaluation board will convert the sine wave CLK input signal to a square wave at TTL logic levels to drive the sample clock input of the HI5667. The ADC data is captured by a logic analyzer and then transferred over the GPIB bus to the PC. The PC has the required software to perform the Fast Fourier Transform (FFT) and do the data analysis.

Coherent testing is recommended in order to avoid the inaccuracies of windowing. The sampling frequency and analog input frequency have the following relationship: $F_I/F_S = M/N$, where F_I is the frequency of the input analog sinusoid, F_S is the sampling frequency, N is the number of samples, and M is the number of cycles over which the samples are taken. By making M an integer and odd number (1, 3, 5, ...) the samples are assured of being nonrepetitive.

Refer to the HI5667 data sheet for a complete list of test definitions and the results that can be expected using the evaluation board with the test setup shown. Evaluating the part with a reconstruction DAC is only suggested when doing bandwidth or video testing.

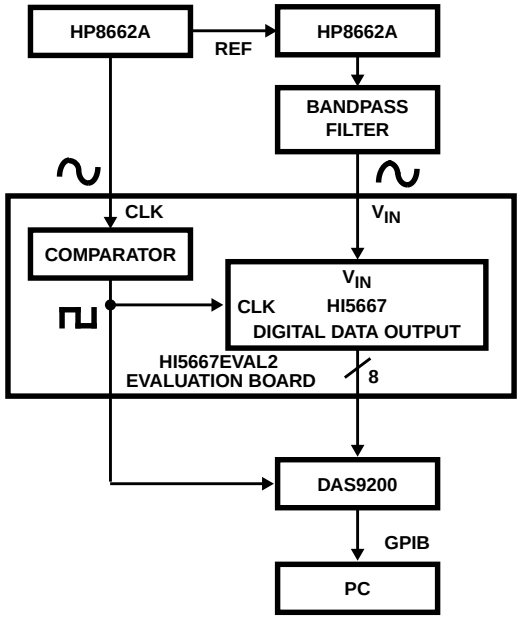


FIGURE 3. HIGH-SPEED A/D PERFORMANCE TEST SYSTEM

Appendix A Board Layout

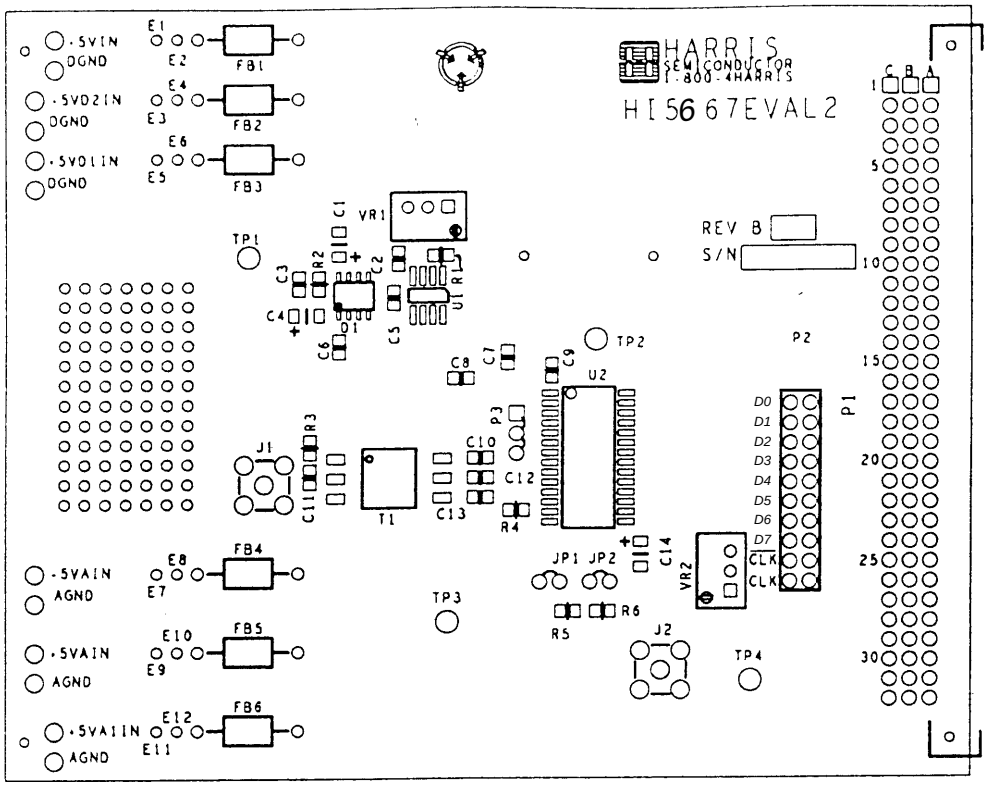


FIGURE 4. HI5667EVAL2 EVALUATION BOARD PARTS LAYOUT (NEAR SIDE)

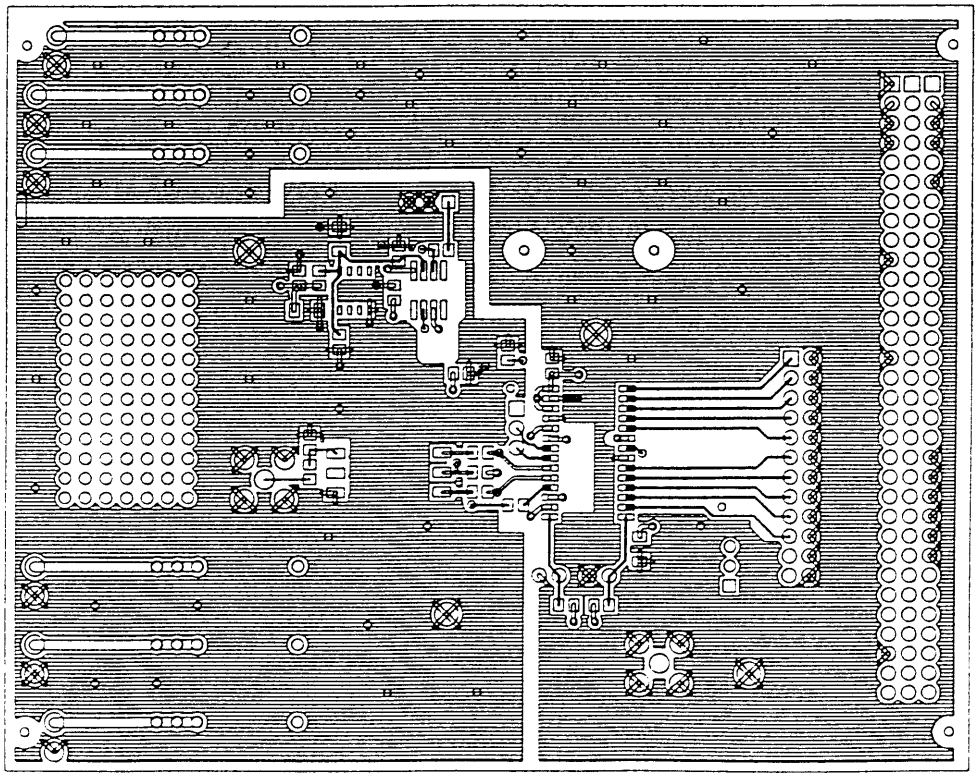


FIGURE 5. HI5667EVAL2 EVALUATION BOARD COMPONENT NEAR SIDE (LAYER 1)

Appendix A Board Layout (Continued)

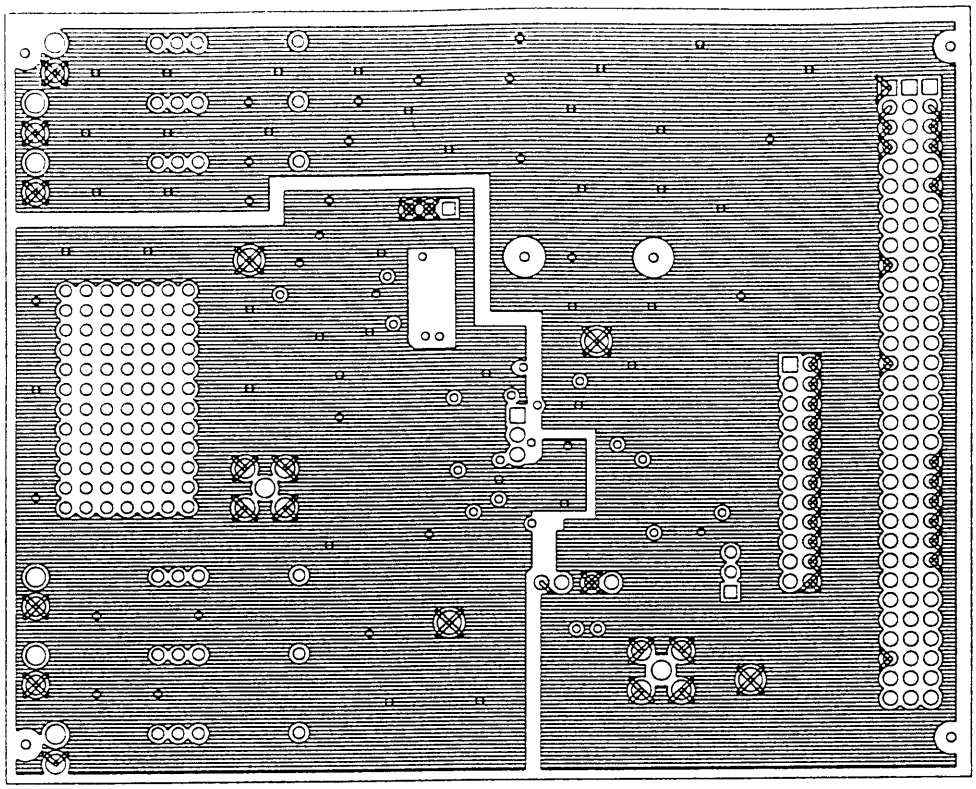


FIGURE 6. HI5667EVAL2 EVALUATION BOARD GROUND PLANE LAYER (LAYER 2)

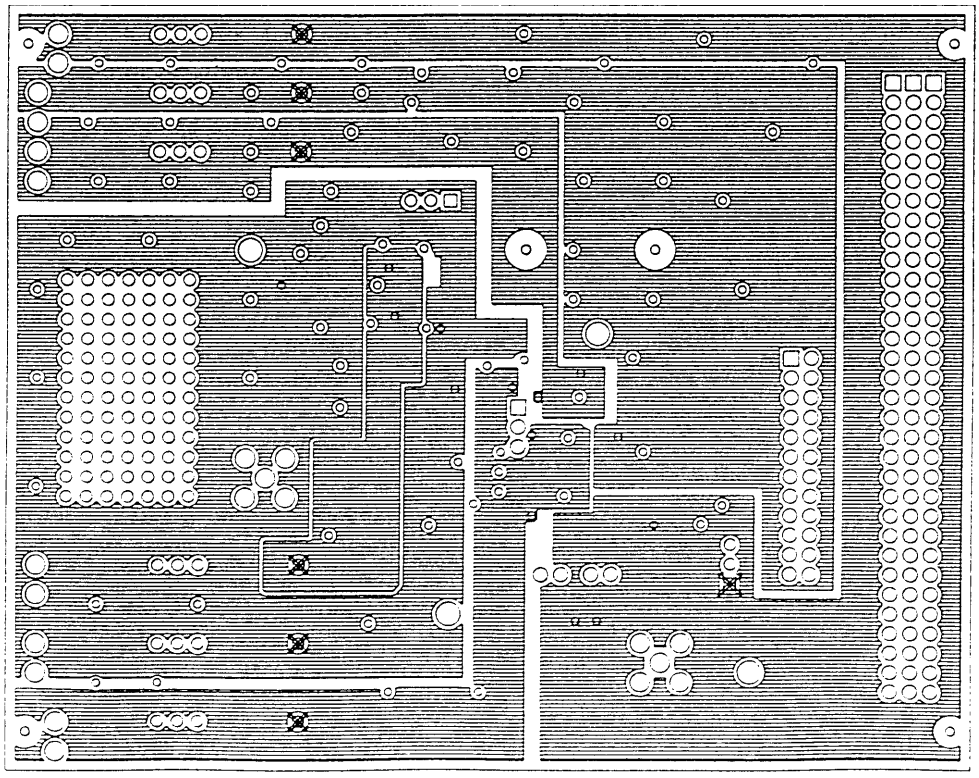


FIGURE 7. HI5667EVAL2 EVALUATION BOARD POWER PLANE LAYER (LAYER 3)

Appendix A Board Layout (Continued)

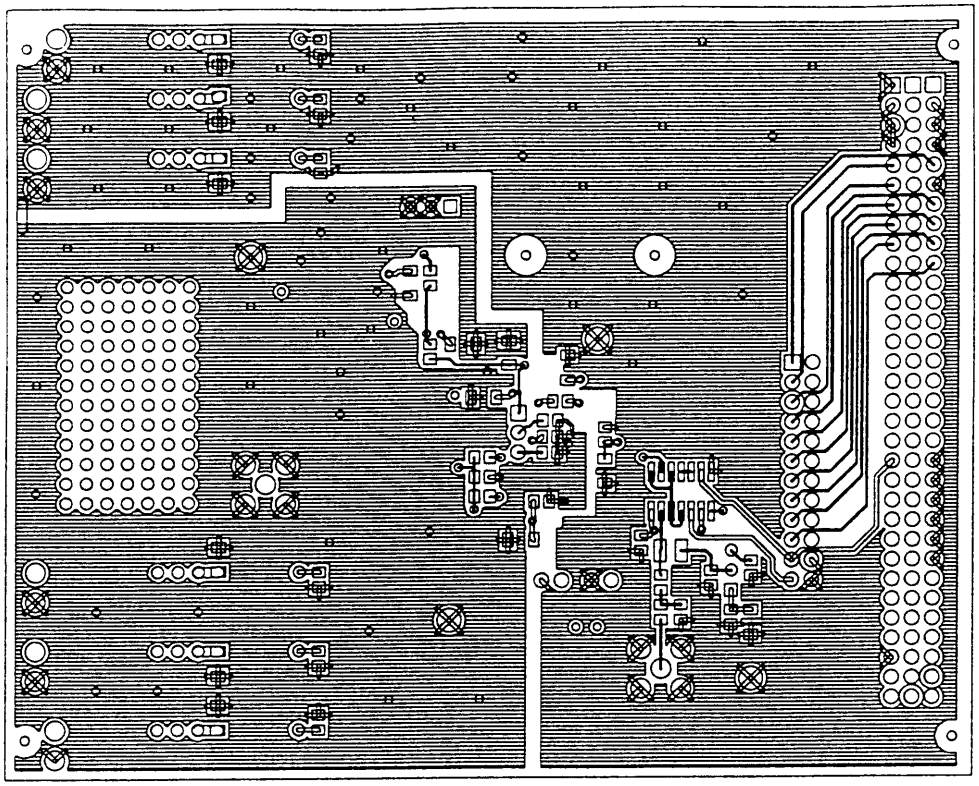


FIGURE 8. HI5667EVAL2 EVALUATION BOARD COMPONENT FAR SIDE (LAYER 4)

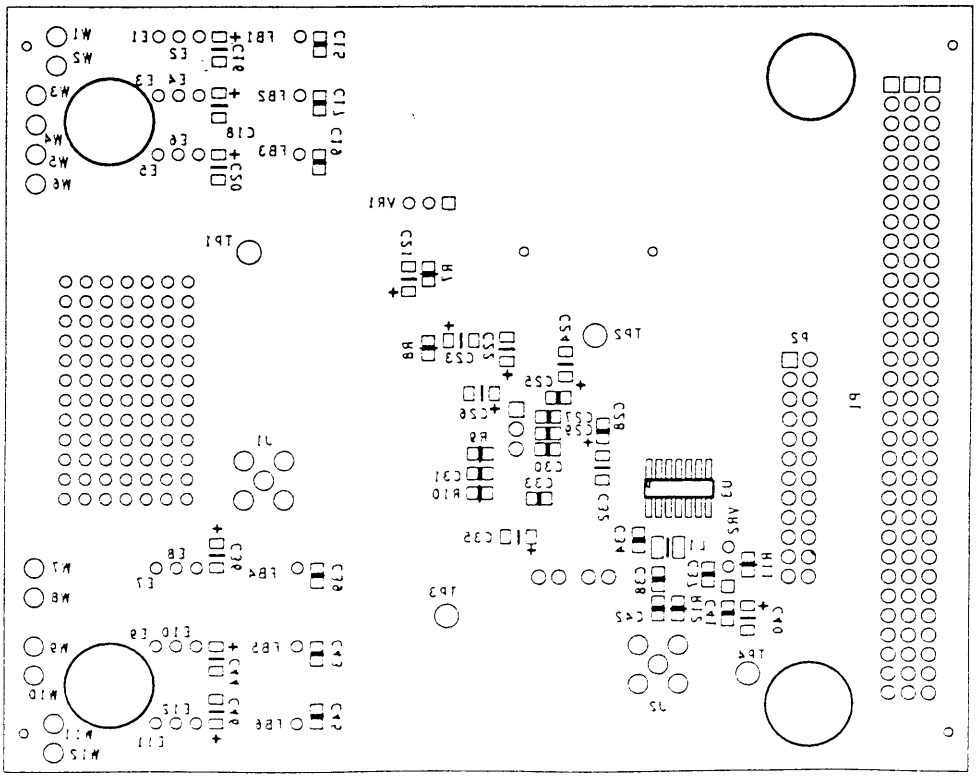
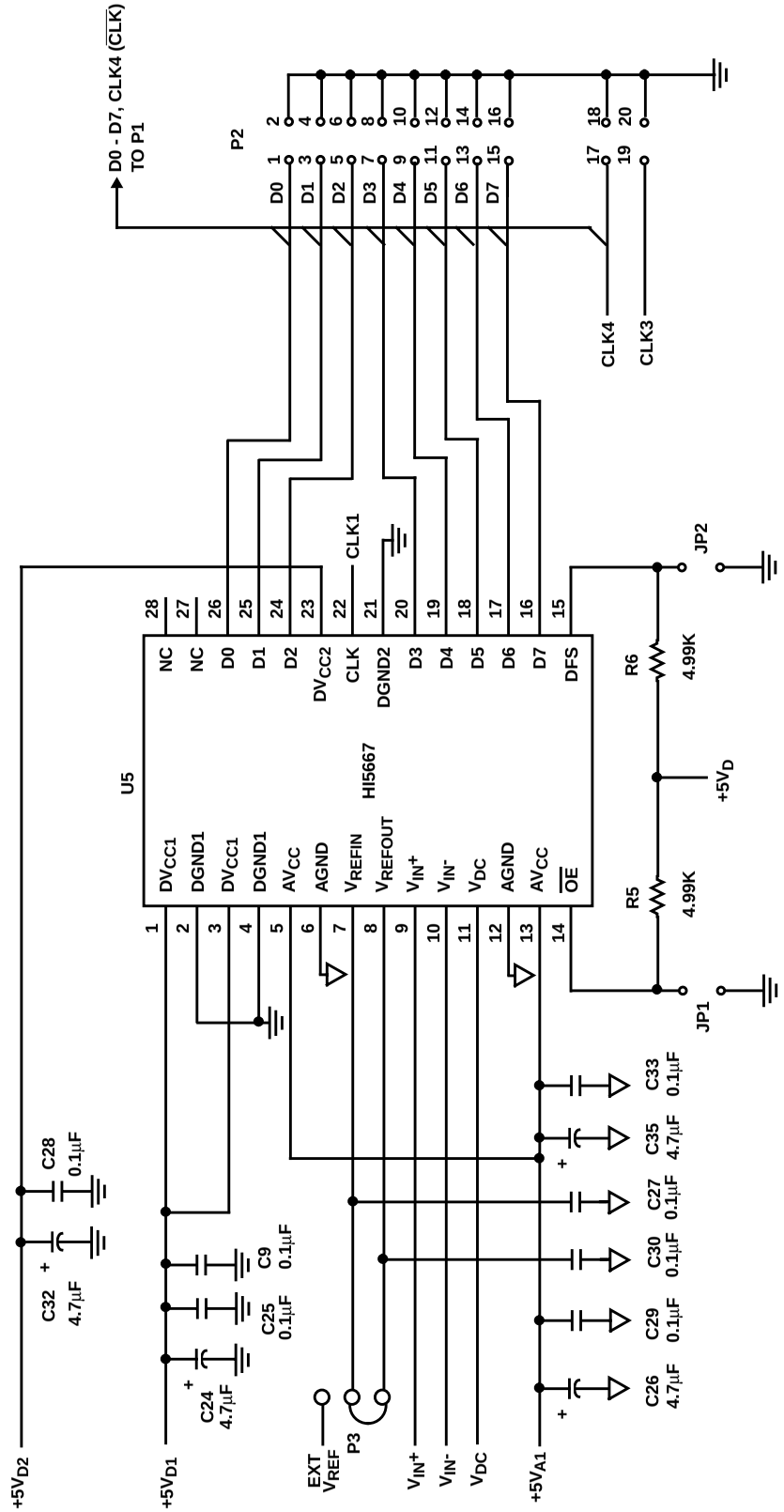
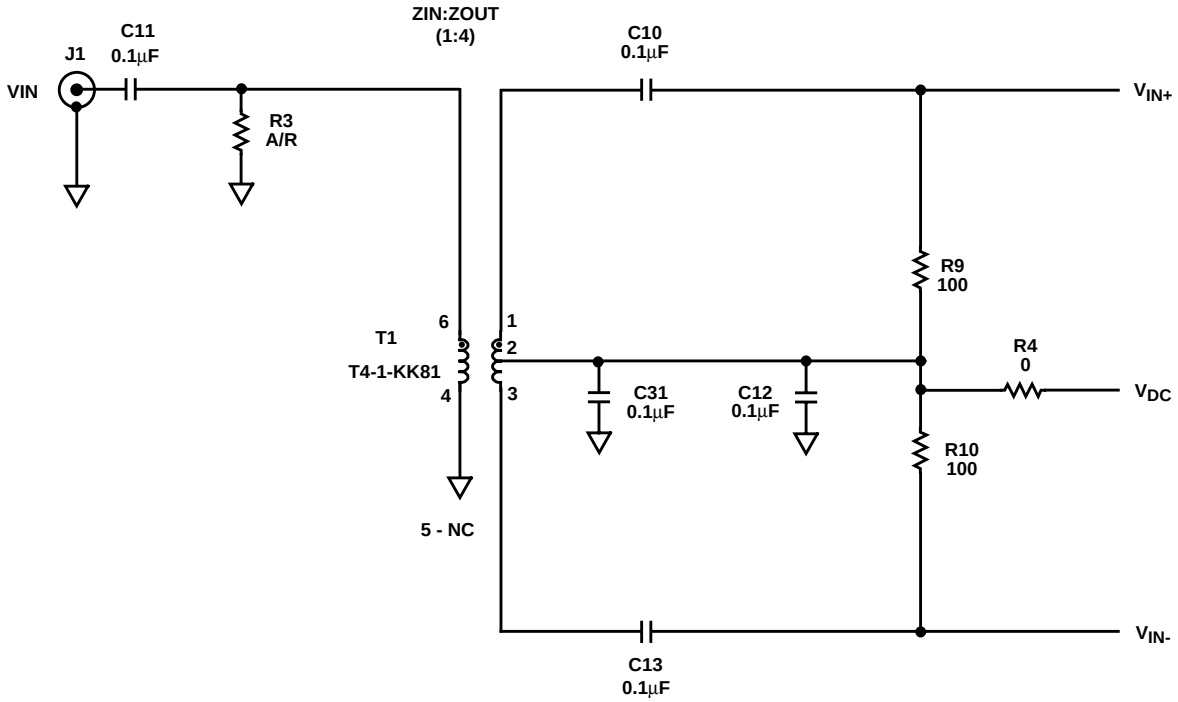


FIGURE 9. HI5667EVAL2 EVALUATION BOARD PARTS LAYOUT (FAR SIDE)

Appendix B Schematic Diagrams

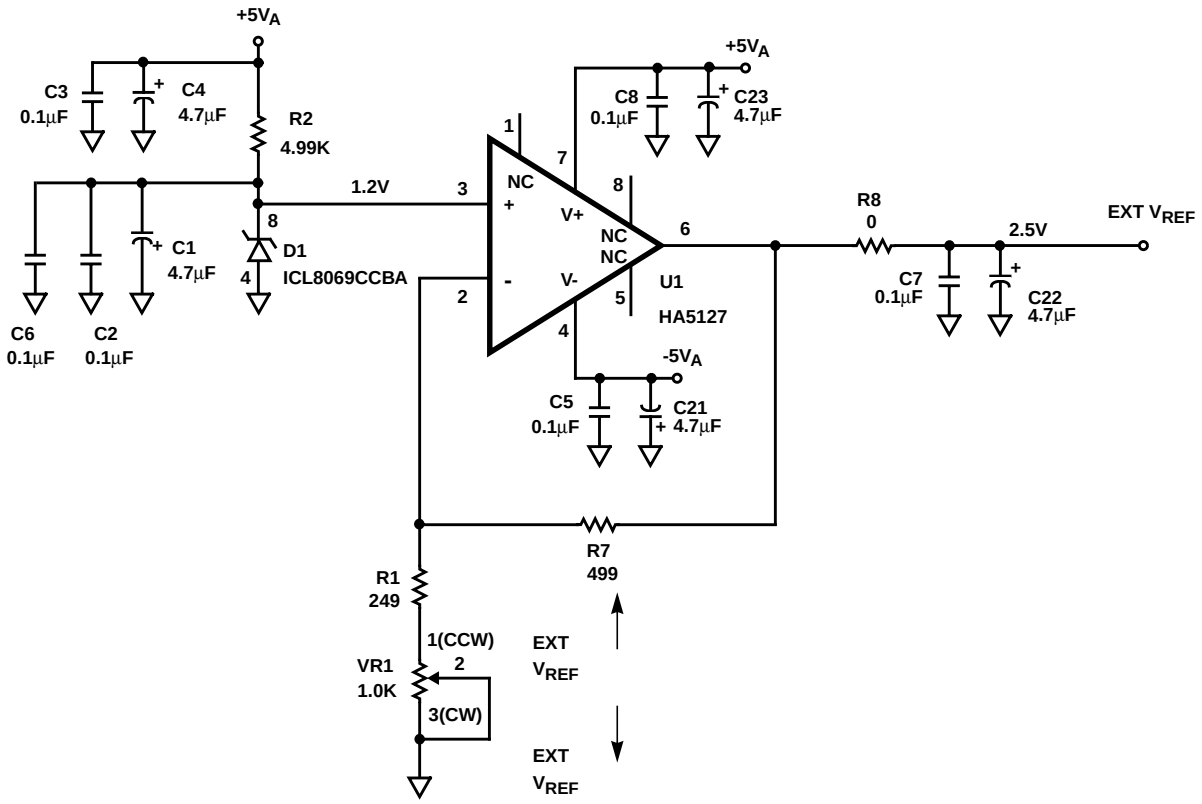


Appendix B Schematic Diagrams (Continued)



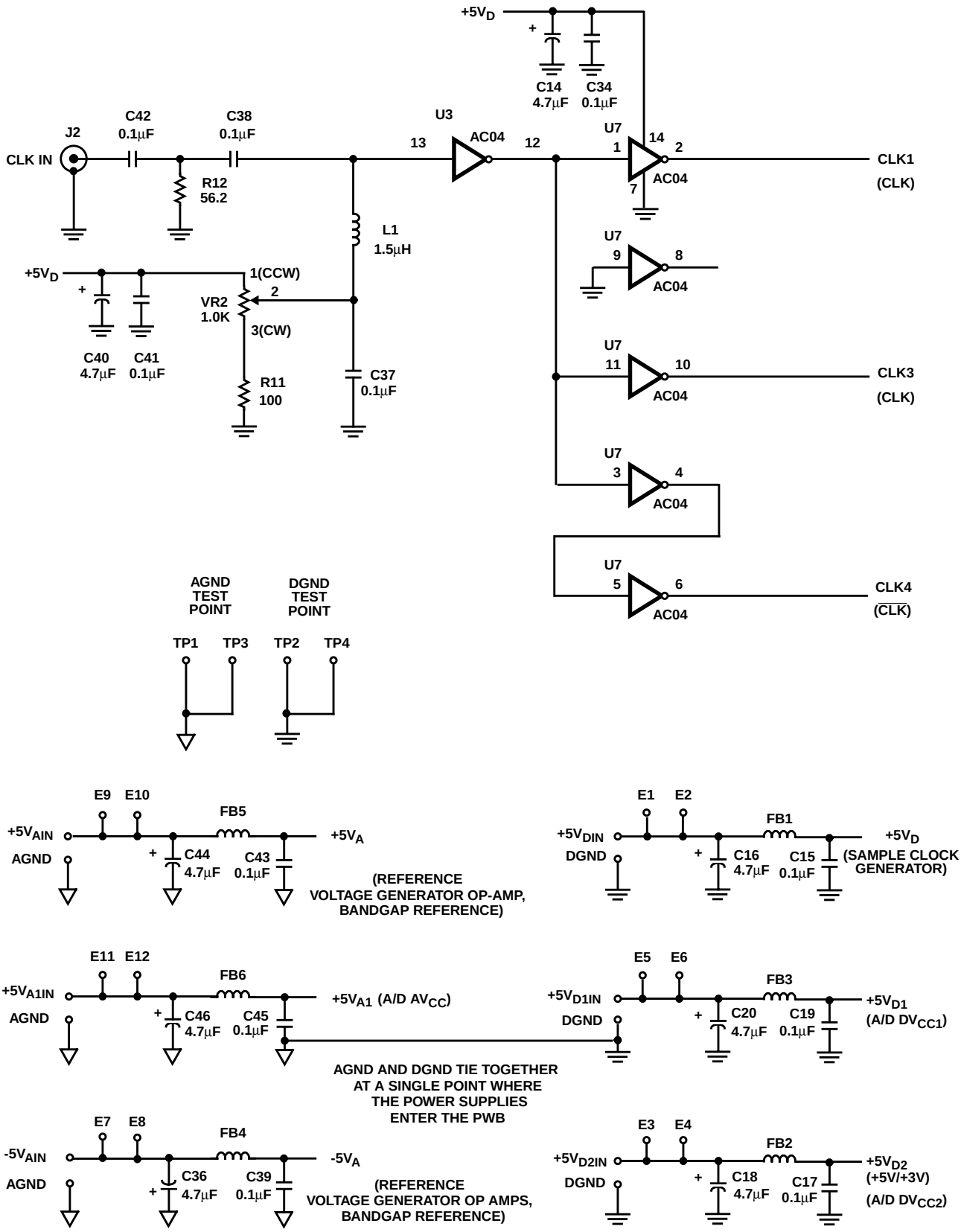
SINGLE-ENDED TO DIFFERENTIAL (TRANSFORMER) ANALOG FRONT END

Appendix B Schematic Diagrams (Continued)

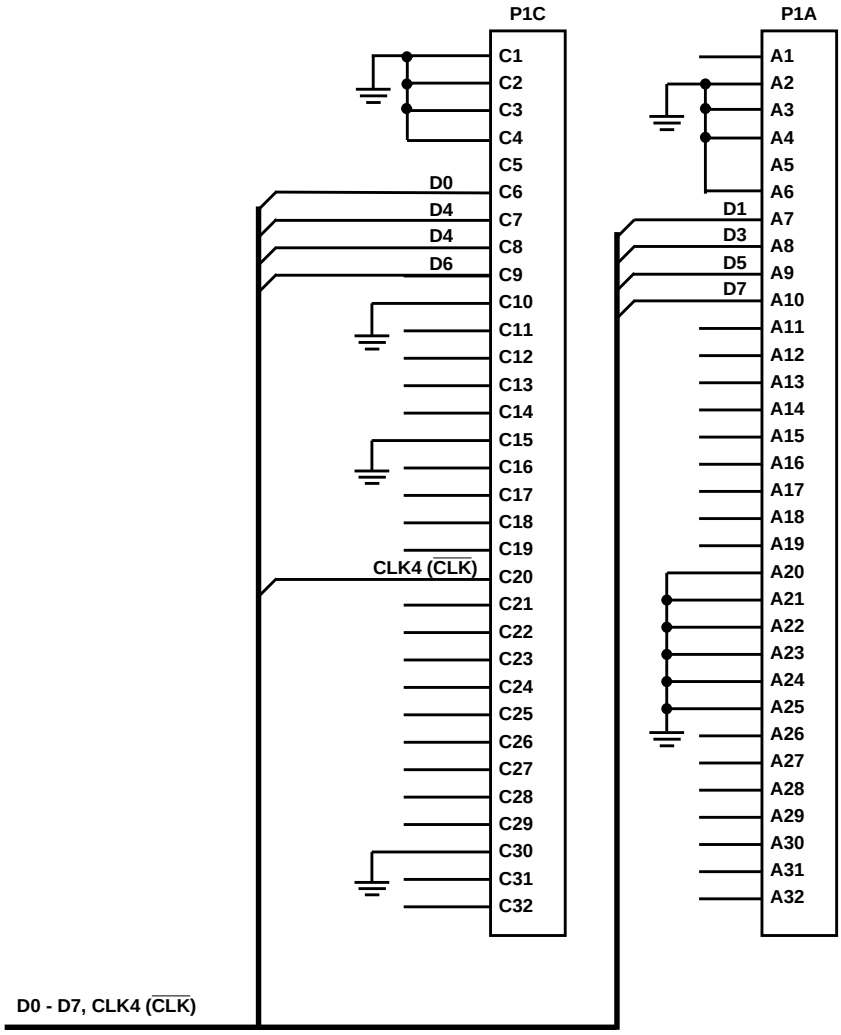


EXTERNAL REFERENCE VOLTAGE GENERATION CIRCUIT

Appendix B Schematic Diagrams (Continued)



Appendix B Schematic Diagrams (Continued)



96 PIN I/O CONNECTOR

Appendix C Parts List

REFERENCE DESIGNATOR	QTY	DESCRIPTION
-	1	Printed Wiring Board
R7	1	499Ω, 1/10W 805 Chip, 1%
R12	1	56.2Ω, 1/10W 805 Chip, 1%
R3	1	A/RΩ, 1/10W 805 Chip, 1%
R9, R10, R11	3	100Ω, 1/10W 805 Chip, 1%
R4, R8	2	0.0Ω, 1/10W 805 Chip, 1%
R2, R5, R6	3	4.99kΩ, 1/4W 805 Chip, 5%
R1	1	249Ω, 1/10W 805 Chip, 1%
VR1, VR2	2	1kΩ Trim Pot
C1, C4, C14, C16, C18, C20, C21, C22, C23, C24, C26, C32, C35, C36, C40, C44, C46	17	4.7µF Chip Tant Cap, 10WVDC, 20%, EIA Case A
C2, C3, C5, C6, C7, C8, C9, C10, C11, C12, C13, C15, C17, C19, C25, C27, C28, C29, C30, C31, C33, C34, C37, C38, C39, C41, C42, C43, C45	29	0.1µF Cer Cap, 50WVDC, 10%, 805 Case, Y5V Dielectric
T1	1	RF Transformer, 1:4 Primary to Secondary Impedance Ratio

REFERENCE DESIGNATOR	QTY	DESCRIPTION
L1	1	1.5µH Chip Inductor, 1210 Case
FB1-6	6	10µH Ferrite Bead
J1, J2	2	SMA Straight Jack PCB Mount
-	4	Protective Bumper
JP1, JP2	2	1x2 Header
JPH1, JPH2	2	1x2 Header Jumper
P3	1	1x3 Header
PH3	1	1x2 Header Jumper
P2	1	2x10 Header
TP1, TP2, TP3, TP4	4	Test Point
U2	1	Intersil HI5667 8-Bit 60MSPS A/D Converter with Internal Voltage Reference
U1	1	Intersil HA9P5127-5 8.5MHz, Ultra-Low Noise Precision Operational Amplifier
U3	1	Intersil CD74HC04M High Speed CMOS Logic Hex Inverter
D1	1	Intersil ICL8069CCBA Low Voltage Bandgap Reference
P1	6	64-Pin Eurocard RT Angle Receptacle

Appendix D HI5667 Theory of Operation

The HI5667 is a 8-bit fully differential sampling pipeline A/D converter with digital error correction logic. Figure 10 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal sampling clock which is a non-overlapping two phase signal, ϕ_1 and ϕ_2, derived from the master sampling clock. During the sampling phase, ϕ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of ϕ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, ϕ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The front end sample-and-hold output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of a switch and C_S. The relatively small values of these components result in a typical full power input bandwidth of 250MHz for the converter.

As illustrated in the functional block diagram, identical pipeline subconverter stages, each containing a two-bit flash converter and a two-bit multiplying digital-to-analog converter, follow the S/H circuit with the last stage being a two bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual subconverter clock signal is offset by 180 degrees from the previous stage clock signal resulting in alternate stages in the pipeline performing the same operation.

The output of each of the identical two-bit subconverter stages is a two-bit digital word containing a supplementary bit to be used by the digital error correction logic. The output of each subconverter stage is input to a digital delay line which is controlled by the internal sampling clock. The function of the digital delay line is to time align the digital outputs of the two-bit subconverter stages with the corresponding output of the last stage flash converter before applying the result to the digital error correction logic. The digital error correction logic uses the supplementary bits to correct any error that may exist before generating the final eight bit digital data output of the converter.

Because of the pipeline nature of this converter, the digital data representing an analog input sample is output to the digital data bus on the 7th cycle of the clock after the analog sample is taken. This time delay is specified as the data latency. After the data latency time, the digital data representing each succeeding analog sample is output during the following clock cycle. The digital output data is synchronized to the external sampling clock by a double buffered latching technique. The digital output data is available in two's complement or offset binary format depending on the state of the Data Format Select (DFS) control input.

Internal Reference Voltage Output, V_{REFOUT}

The HI5667 is equipped with an internal reference voltage generator, therefore, no external reference voltage is required. V_{REFOUT} must be connected to V_{REFIN} when using the internal reference voltage.

An internal band-gap reference voltage followed by an amplifier/buffer generates the precision +2.5V reference voltage used by the converter. A 4:1 array of substrate PNPs generates the "delta-V_{BE}" and a two-stage op amp closes the loop to create an internal +1.25V band-gap reference voltage. This voltage is then amplified by a wide-band uncompensated operational amplifier connected in a gain-of-two configuration. An external, user-supplied, 0.1µF capacitor connected from the V_{REFOUT} output pin to analog ground is used to set the dominant pole and to maintain the stability of the operational amplifier.

Reference Voltage Input, V_{REFIN}

The HI5667 is designed to accept a +2.5V reference voltage source at the V_{REFIN} input pin. Typical operation of the converter requires V_{REFIN} to be set at +2.5V. The HI5667 is tested with V_{REFIN} connected to V_{REFOUT} yielding a fully differential analog input voltage range of ±0.5V.

The user does have the option of supplying an external +2.5V reference voltage. As a result of the high input impedance presented at the V_{REFIN} input pin, 2.5kΩ typically, the external reference voltage being used is only required to source 1mA of reference input current. In the situation where an external reference voltage will be used an external 0.1µF capacitor **must** be connected from the V_{REFOUT} output pin to analog ground in order to maintain the stability of the internal operational amplifier.

In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at the reference voltage input pin, V_{REFIN}.

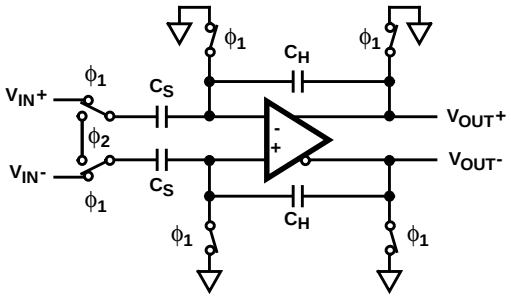
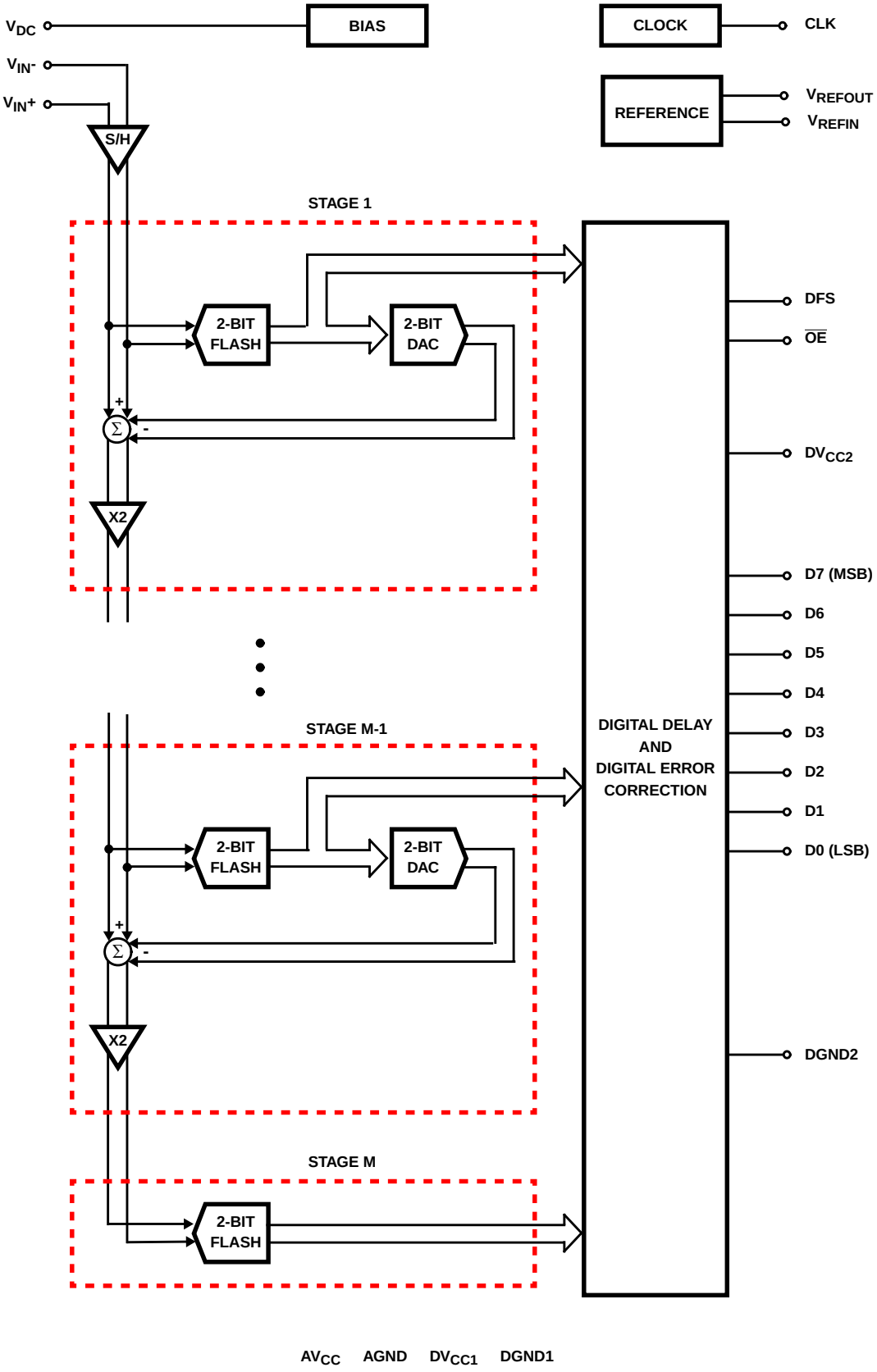


FIGURE 10. ANALOG INPUT SAMPLE-AND-HOLD

HI5667 Functional Block Diagram



Appendix E Pin Descriptions

PIN #	NAME	DESCRIPTION
1	DV_{CC1}	Digital Supply (+5.0V)
2	DGND1	Digital Ground
3	DV_{CC1}	Digital Supply (+5.0V)
4	DGND1	Digital Ground
5	AV_{CC}	Analog Supply (+5.0V)
6	AGND	Analog Ground
7	V_{REFIN}	+2.5V Reference Voltage Input
8	V_{REFOUT}	+2.5V Reference Voltage Output
9	$V_{IN}+$	Positive Analog Input
10	$V_{IN}-$	Negative Analog Input
11	V_{DC}	DC Bias Voltage Output
12	AGND	Analog Ground
13	AV_{CC}	Analog Supply (+5.0V)
14	$\overline{OE}$	Digital Output Enable Control Input
15	DFS	Data Format Select Input
16	D7	Data Bit 7 Output (MSB)
17	D6	Data Bit 6 Output
18	D5	Data Bit 5 Output
19	D4	Data Bit 4 Output
20	D3	Data Bit 3 Output
21	DGND2	Digital Ground
22	CLK	Sample Clock Input
23	DV_{CC2}	Digital Output Supply (+3.0V or +5.0V)
24	D2	Data Bit 2 Output
25	D1	Data Bit 1 Output
26	D0	Data Bit 0 Output
27	NC	No Connection
28	NC	No Connection

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